UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
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ART UNIT	PAPER NUMBER
2186	8

DATE MAILED: 10/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _21 August 2003_ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-17_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-17_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application (PTO-152)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	6) ☐ Other:

Detailed Action

1.   Claims 1-17 are presented for examination.   This office action is in response to the

amendment filed on 8/21/03.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before
> the invention by the applicant for patent, except that an international application filed under the treaty
> defined in section 351(a) shall have the effect under this subsection of a national application published
> under section 122(b) only if the international application designating the United States was published under
> Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by
> the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes
> of this subsection based on the filing of an international application filed under the treaty defined in section
> 351(a).

3.   Claims 1-4, 6-12, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by

Shen et al. (Shen) U.S. Patent 6,526,481.

As to claim 1 , Shen discloses the invention as claimed. Shen discloses a cache-coherent

device comprising (Fig. 1): a plurality of client ports (Fig. 1 Refs. 130's), each to be coupled to

one of a plurality of port components (Fig. 1 Refs. 110); a plurality of sub-unit caches (Fig. 2

Refs. 134), each coupled to one of said plurality of client ports and assigned to one of said

plurality of port components; and a coherency engine (Fig. 2 Refs. 132 & 140) coupled to said

plurality of sub-unit caches.

As to claim 2, Shen discloses the invention as claimed in the above. Shen further

discloses wherein said plurality of port components include processor port components (Fig. 1

Ref. 110).

As to claim 3, Shen discloses the invention as claimed in the above. Shen further

discloses wherein said plurality of port components include input/output components (Fig. 1 Ref.

110).

As to claim 4, Shen discloses the invention as claimed in the above. Shen further

discloses wherein said plurality of sub-unit caches include transaction buffers using a coherency

logic protocol (Fig. 2 Refs. 132 & 140).

As to claim 6 , Shen discloses the invention as claimed. Shen discloses a cache-

processing system comprising (Fig. 1) : a processor (Fig. 1 Ref 110); a plurality of port

components (Fig. 1 Ref. 110); and a cache-coherent device (Fig. 2 Refs. 132 & 140) coupled to

said processor and including a plurality of client ports (Fig. 2 Ref. 130), each coupled to one of

said plurality of port components (Fig. 1 Ref. 110), said cache-coherent device further including

a plurality of caches (Fig. 2 Ref. 134), each coupled to one of said plurality of client ports and

assigned to one of said plurality of port components, and a coherency engine (Fig. 2 Fig. 140)

coupled to said plurality of caches.

As to claim 7, Shen discloses the invention as claimed in the above. Shen further

discloses wherein said plurality of port components include processor port components (Fig. 1

Ref. 110).

As to claim 8, Shen discloses the invention as claimed in the above. Shen further

discloses wherein said plurality of port components include input/output components (Fig. 1 Ref.

Ref. 110).

As to claim 9 , Shen discloses the invention as claimed. Shen discloses in a cache-

coherent device (Fig. 1) including a coherency engine (Fig. 2 Refs. 132 & 140) and a plurality of

client ports (Fig. 1 Refs 130), a method for processing a transaction, comprising: receiving a

transaction request (col. 7 lines 13-15) at one of said plurality of client ports, said transaction

request includes an address (col. 8 line 49); and determining whether said address is present (col.

8 lines 45+) in one of a plurality of sub-unit caches (Fig. 2 Ref. 134), each of said sub-unit caches

assigned to said of a plurality of client ports (Fig. 2 Ref. 110).

As to claim 10, Shen discloses the invention as claimed in the above. Shen further

discloses wherein said transaction request is a read transaction request (col. 7 lines 13-15).

As to claim 11, Shen discloses the invention as claimed in the above. Shen further

discloses transmitting data for said read transaction request from said one of said plurality of sub-

unit caches to one of said plurality of client ports (col. 8 lines 45+).

As to claim 12, Shen discloses the invention as claimed in the above. Shen further

discloses prefetching one or more cache lines ahead of said read transaction request (cache

memory reads on this limitation since the cache memory is used to assure that the currently

useful data of main memory are copied into the small and fast cache for the purpose of increasing

data access speed by means of spacial and temporal localities); and updating the coherency state

(Col. 9 lines 5-6) information in said plurality of sub-unit caches.

As to claim 14, Shen discloses the invention as claimed in the above. Shen further

discloses wherein said transaction request is a write transaction request (col. 7 lines 13-15).

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth
> in section 102 of this title, if the differences between the subject matter sought to be patented and the prior
> art are such that the subject matter as a whole would have been obvious at the time the invention was made

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 5, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (Shen) U.S. Patent 6,526,481 in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp 140-240.

As to claims 5 and 13, Shen discloses the invention as claimed above. However Shen does not specifically disclose wherein said coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol.

However, it is well known in the cache art to using MESI cache coherency protocol for the purpose of maintaining data consistency thereby increasing the memory access speed. For example, Handy discloses coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol of Handy into the invention of Shen for the advantages stated above.

As to claim 15, Shen and Handy disclose the invention as claimed in the above. Handy further discloses modifying coherency state information for a cache line in said one of said plurality of sub-unit caches; updating coherency state information in others of said plurality of sub-unit caches by said coherency engine; and transmitting data for said write transaction

request from said one of said plurality of sub-unit caches to memory (MESI protocol reads on

this limitation and pages 159-161).

6.   Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al.

(Shen) U.S. Patent 6,526,481 in view of Jim Handy, "The Cache Memory Handbook"

TK7895.M4H35, 1993, pp 140-240 and further in view of Witt et al. (Witt) U.S. Patent

6,202,139.

As to claim 16, Shen further discloses modifying coherency state information of said

write transaction request (col. 7 line 13-15), however, neither Shen nor Handy specifically

discloses write transaction request in the order received and pipelining multiple write requests.

Witt discloses write transaction request in the order received and pipelining multiple

write requests (col. 2 lines 42-43) for the purpose of avoiding bank conflicts thereby decreasing

the performance losses and increasing the access speed (col. 2 lines 43-45).

Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to incorporate write transaction request in the order received and

pipelining multiple write requests as shown in Witt into the combined invention of Shen and

Handy because it would avoid bank conflicts thereby decreasing the performance losses and

increasing the access speed.

As to claim 17, Shen, Handy and Witt disclose the invention as claimed in the above.

Handy further discloses wherein the coherency state information includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.   See attached PTO-892.

8.   a shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

9.   When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections.   See 37 C.F.R. § 1.111(c).

10.   When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

11.   Any inquiry concerning this communication or earlier communications from the

Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The

Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's

supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be

directed to the Group receptionist whose telephone number is (703) 305-3900.

12.   **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
After-Final   (703) 746-7238
Official   (703) 746-7239 (for formal communications intended for
entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please
label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal
Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
October 24, 2003